Through-Silicon-Via Inductor based DC-DC Converters: The Marriage of the Princess and the Dragon

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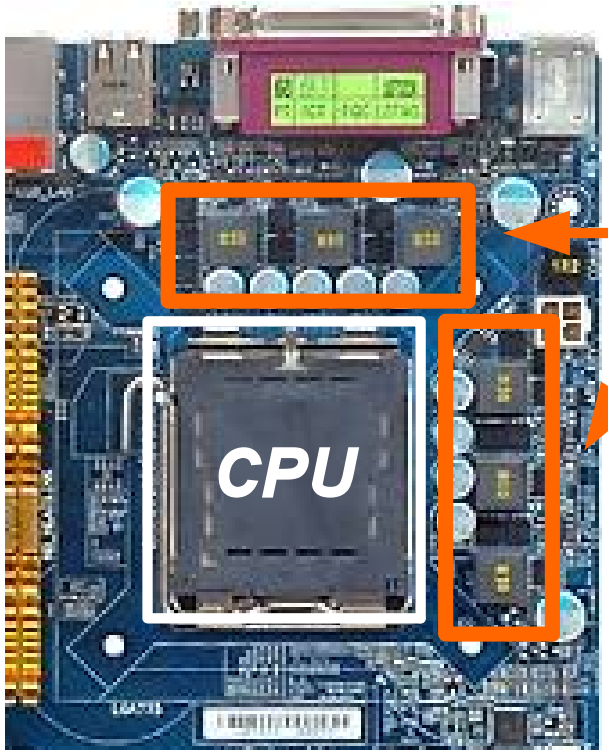
3D ICs
Inductive DC-DC Converters

Limitations of Off-Chip Regulators



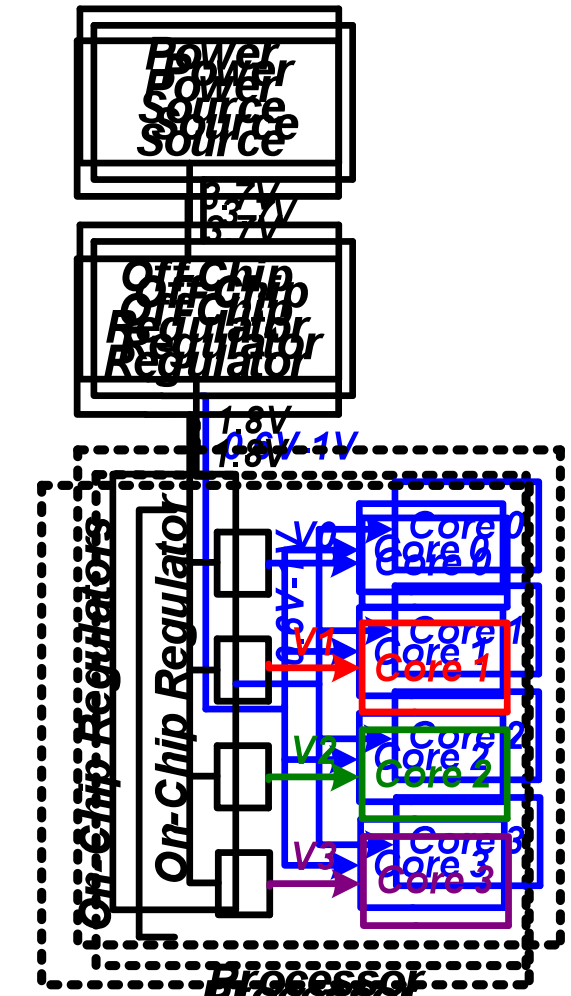
Voltage Regulator

http://www.tomshardware.com
Gigabyte GA-P35C-DS3R

Large Form Factor
Large resonant voltage swings due to package parasitics
External environmental effects

Source: .Gu-Yeon Wei et.al @ Harvard

Power Delivery Schemes



Source: .Gu-Yeon Wei et.al @ Harvard

On-Chip DC-DC Converter Designs

- Linear converters
  - low area overhead
  - Efficiency drops rapidly with the increased load or input/output voltage difference
- Capacitive converters
  - can work for large input/output voltage difference
  - Efficiency still limited to relatively low current loads
- Inductive converters
  - Efficiency increases with load
  - Large area overhead to implement inductors

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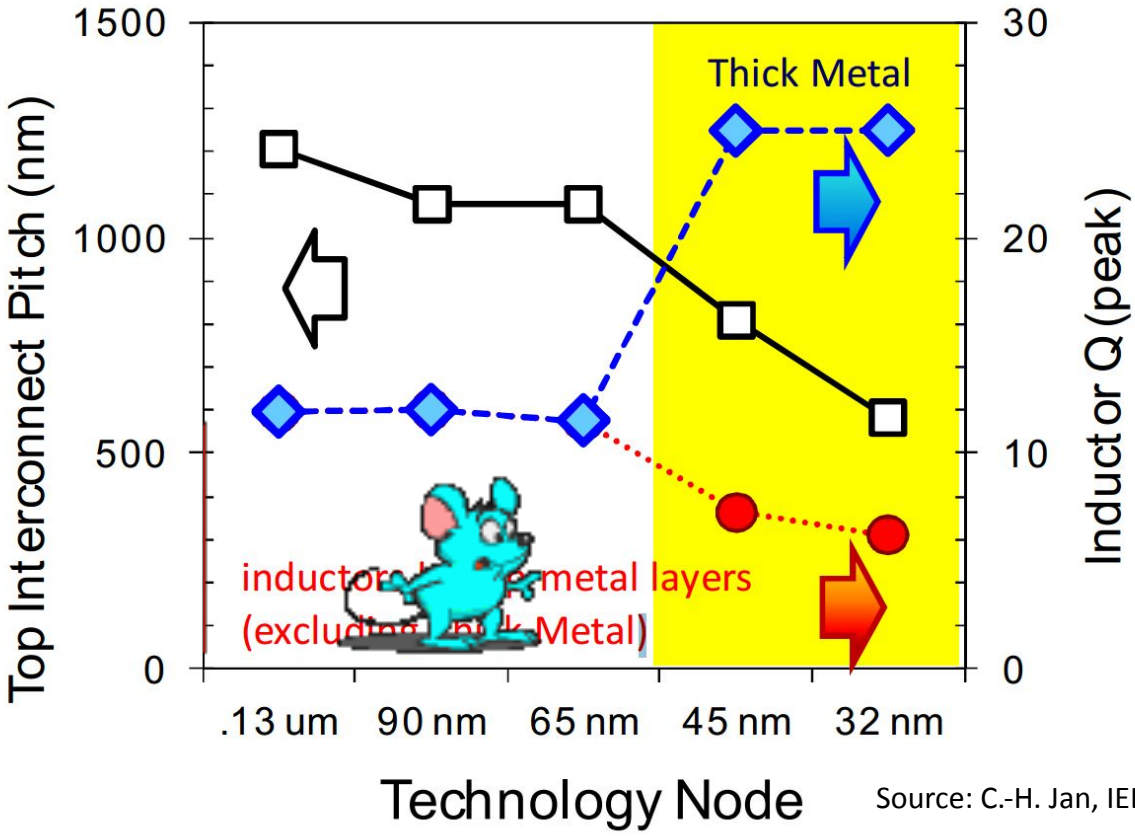
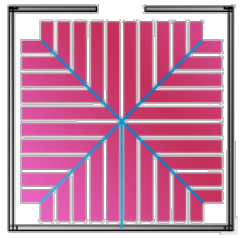
Curse #1: Inductor Scaling



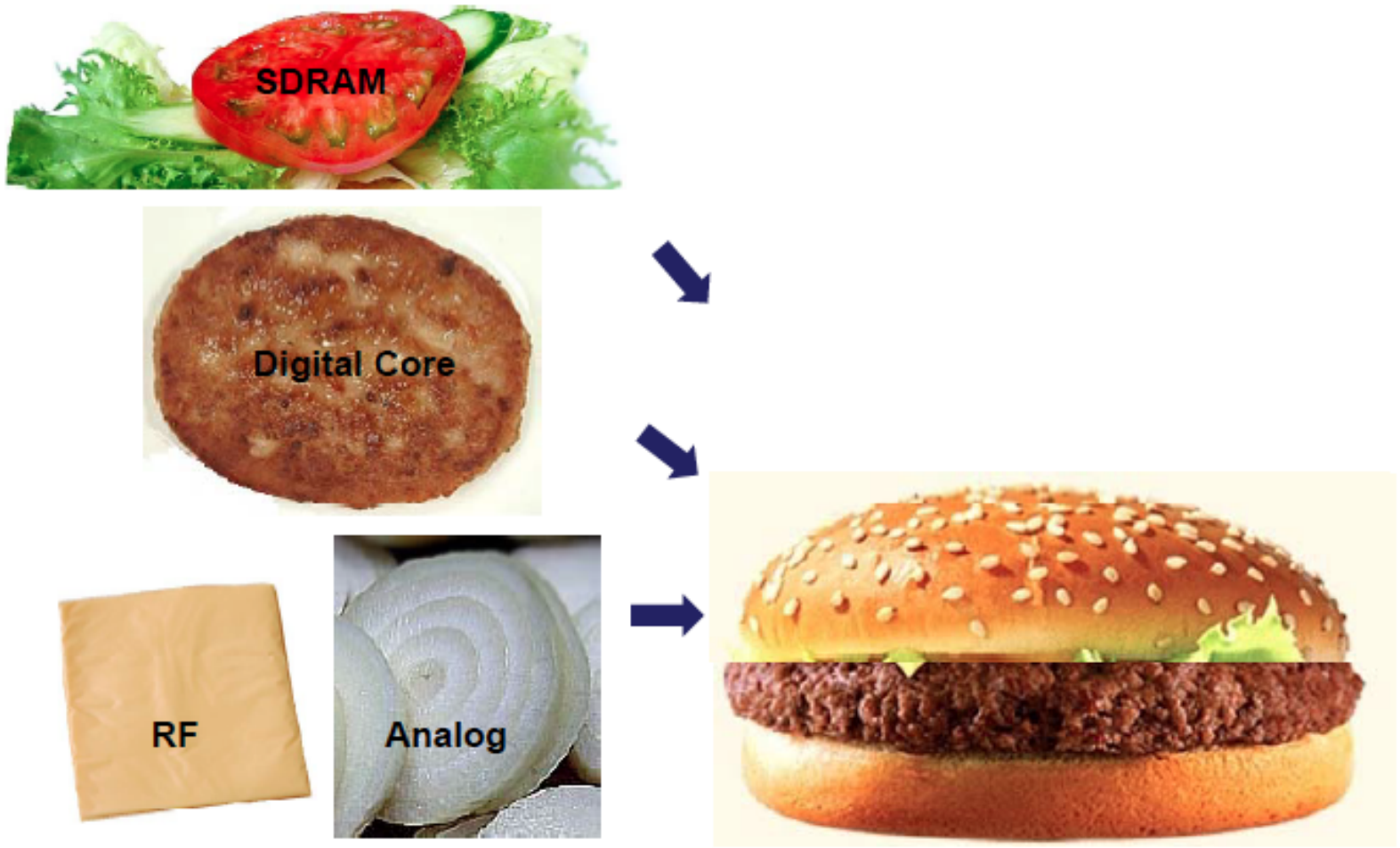
Source: C.-H. Jan, IEDM'10



Patterned ground shield

Brought by scaling of the interconnect pitch and metal thickness

3D Integrated Circuits – the Hamburger

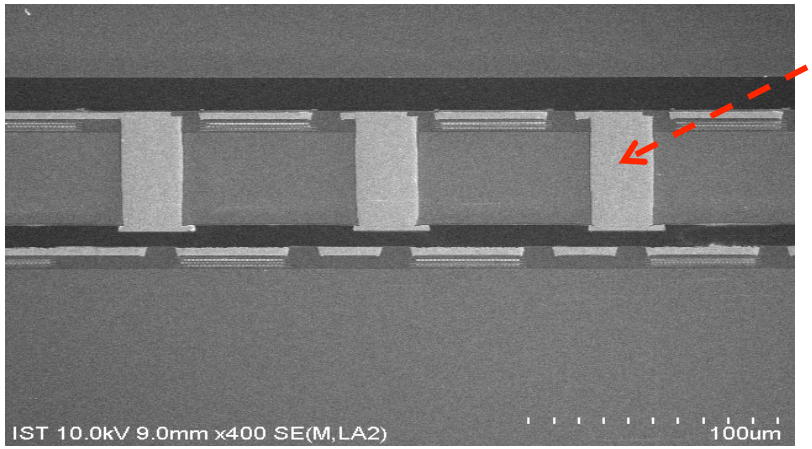


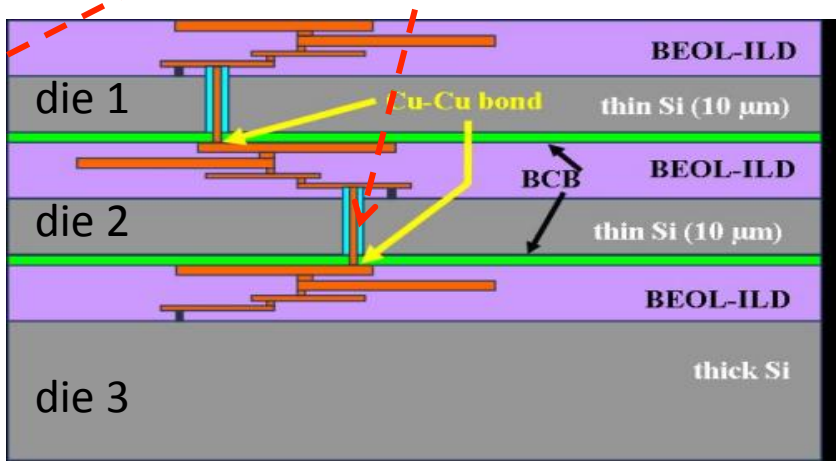
Credit: Joungho Kim @ KAIST

3D Integrated Circuits

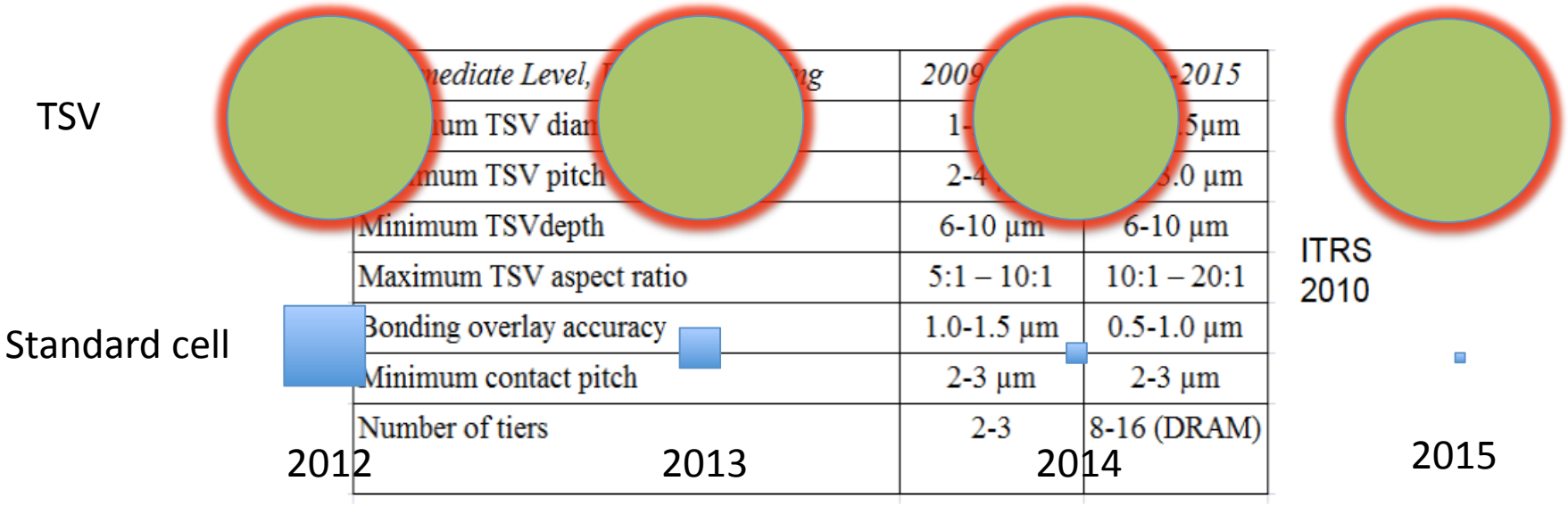
- 3D IC is considered one of the most promising alternatives at the limit of device scaling
  - *Reduced* form factor
  - *Reduced* interconnect length
  - *Compatible* with current technology
  - *Heterogeneous* integration

through-silicon vias (TSVs) for vertical signal link





Curse #2: TSV Scaling



mediate Level, ng	*2009*	*-2015*
um TSV dian	1-	5µm
mum TSV pitch	2-4	.0 µm
Minimum TSVdepth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)

Example: 3D-MAPS [Georgia Tech]

✓ TSV scaling limited by the wafer handling and alignment accuracy

50,180 TSVs

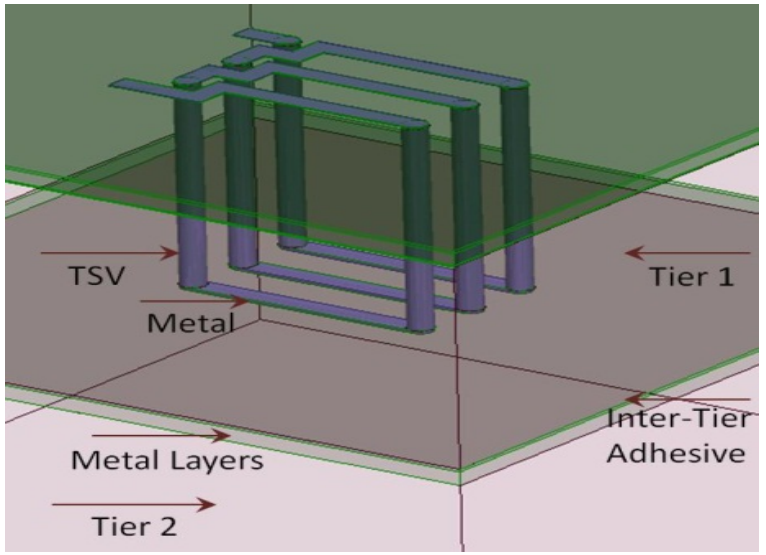
985, 231 um^2 (3.9% total chip area in 130 nm)

If the chip would be re-designed in 17 nm technology in 2015, TSV would occupy more than 70% of the area

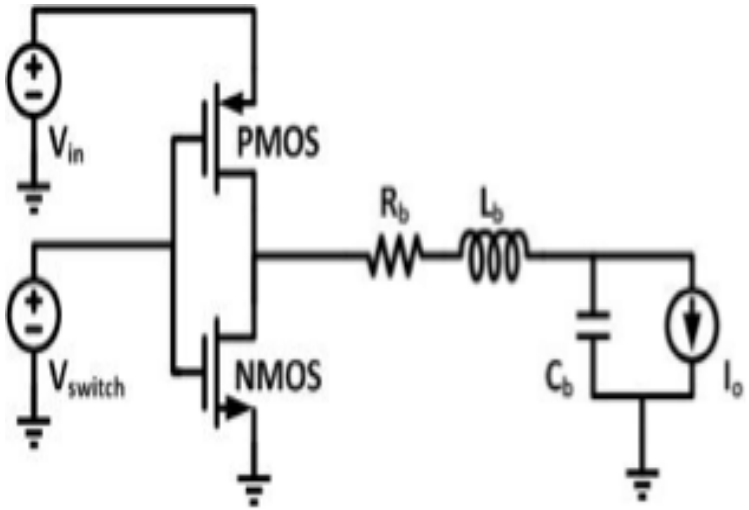
How about On-Chip Converters in 3D ICs?

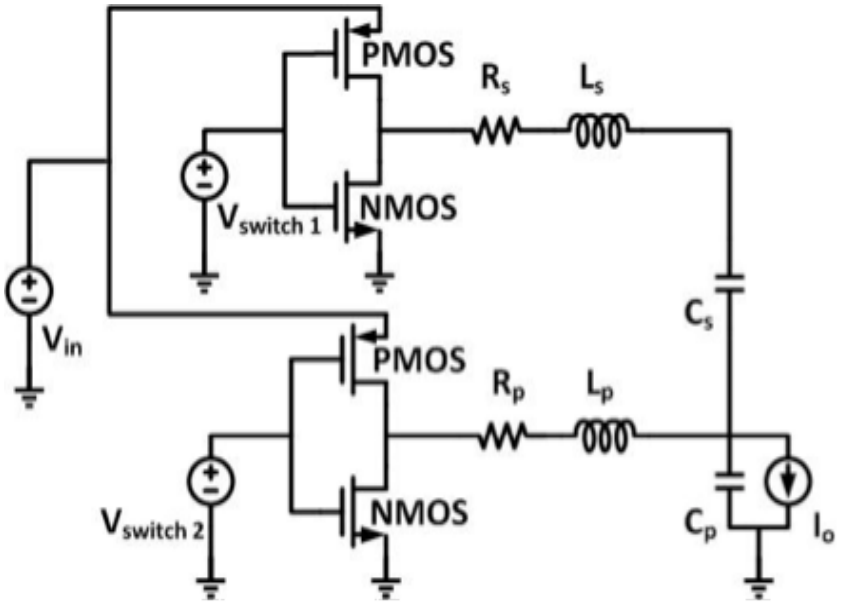
- Subject to both curses?

  - Not necessarily!
- Use dummy TSVs to make inductors
  - Minimum footprint
  - No special RF process
  - Sounds fancy, but…
- Will it work?
  - New loss mechanism?
  - No patterned ground shield?
  - New design freedom?



Inductive Converter Designs





Buck converter

- Easier to implement
- Large ripple

Interleaved converter

- Complex implementation
- Reduced ripple

Outline

- TSV Inductors 101
- On-Chip Inductor Designs
  - Single Inductor Structure
    - Conventional Spiral Inductor
    - Toroidal TSV Inductor
    - Vertical Spiral TSV Inductor
  - Coupled Inductor Pair Structure
    - Conventional Stacked Inductor Pair
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- Circuit Designs and Simulations
  - Buck converter
  - Interleaved converter
- Conclusions

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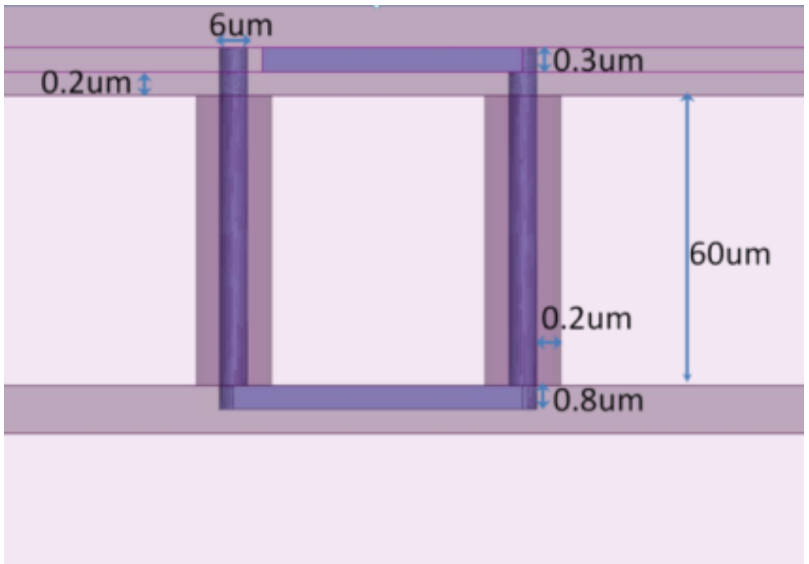
Parameters of Interest

- Process Parameters
  - Substrate Height (H)
  - Conductivity (σ)
  - Diameter (D)
  - Liner Thickness (d)
- Design Parameters
  - Number of Turns (N)
  - Number of Tiers (T)
  - Metal width (W)
  - Loop Pitch (P)
  - Frequency (f)

DOE with nominal settings

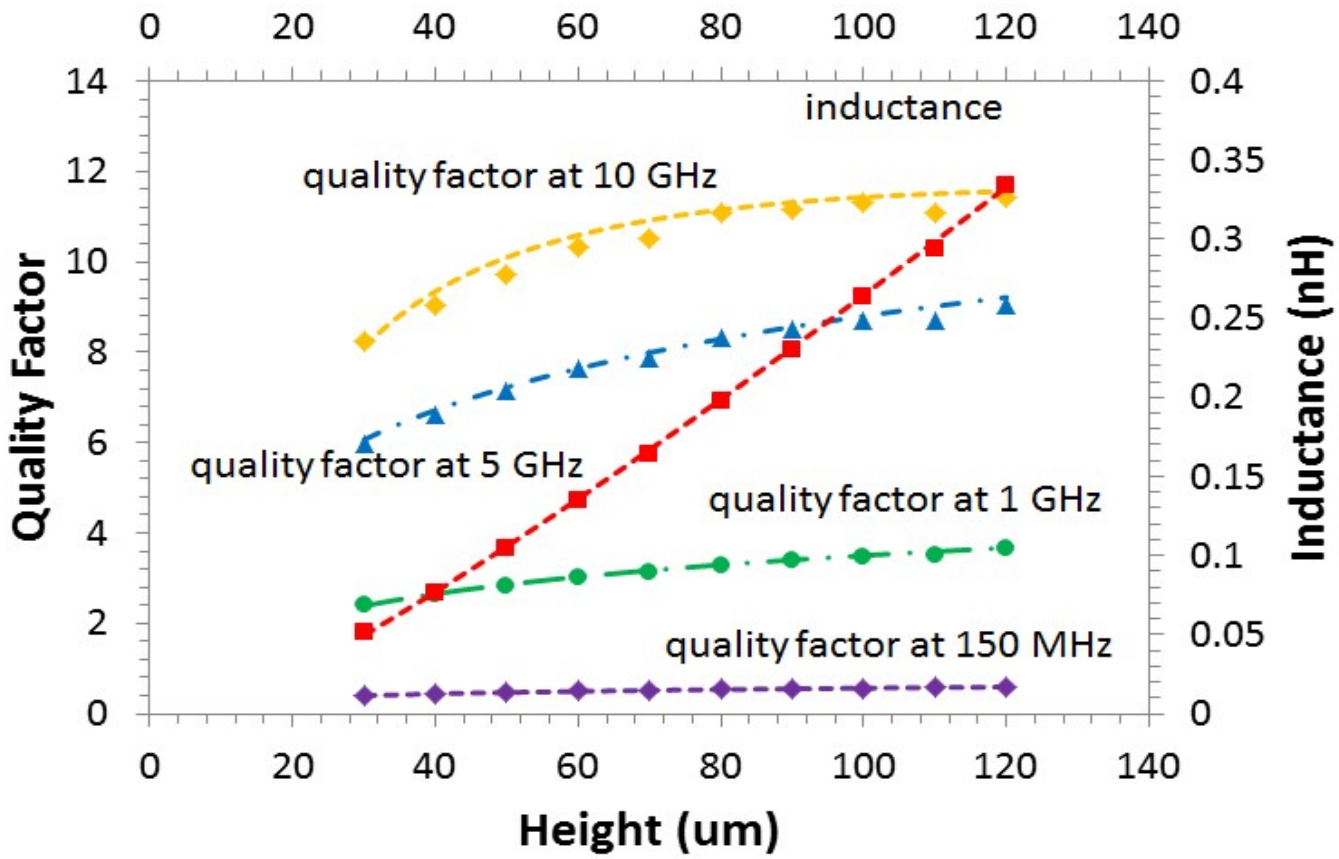


P=18um, W=6um,
f=0.15, 1, 5, 10 GHz

voltage regulators

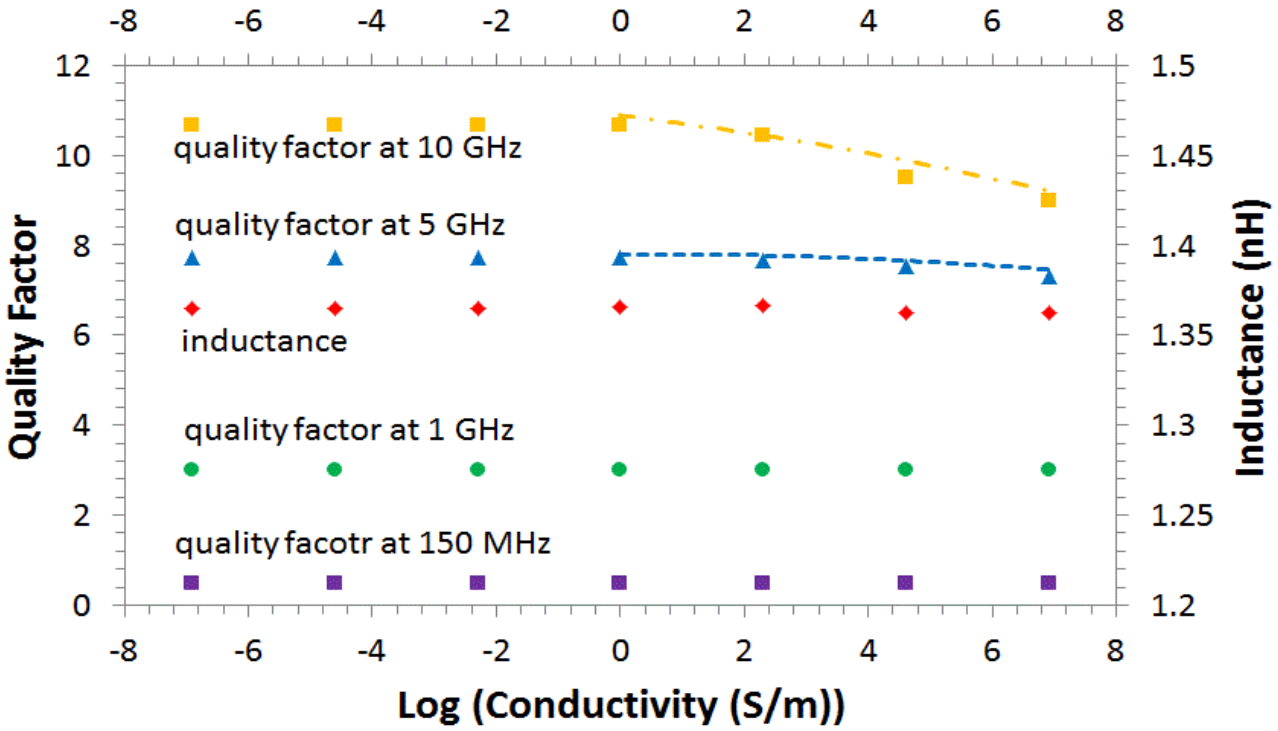
RF applications

Substrate Height (H)



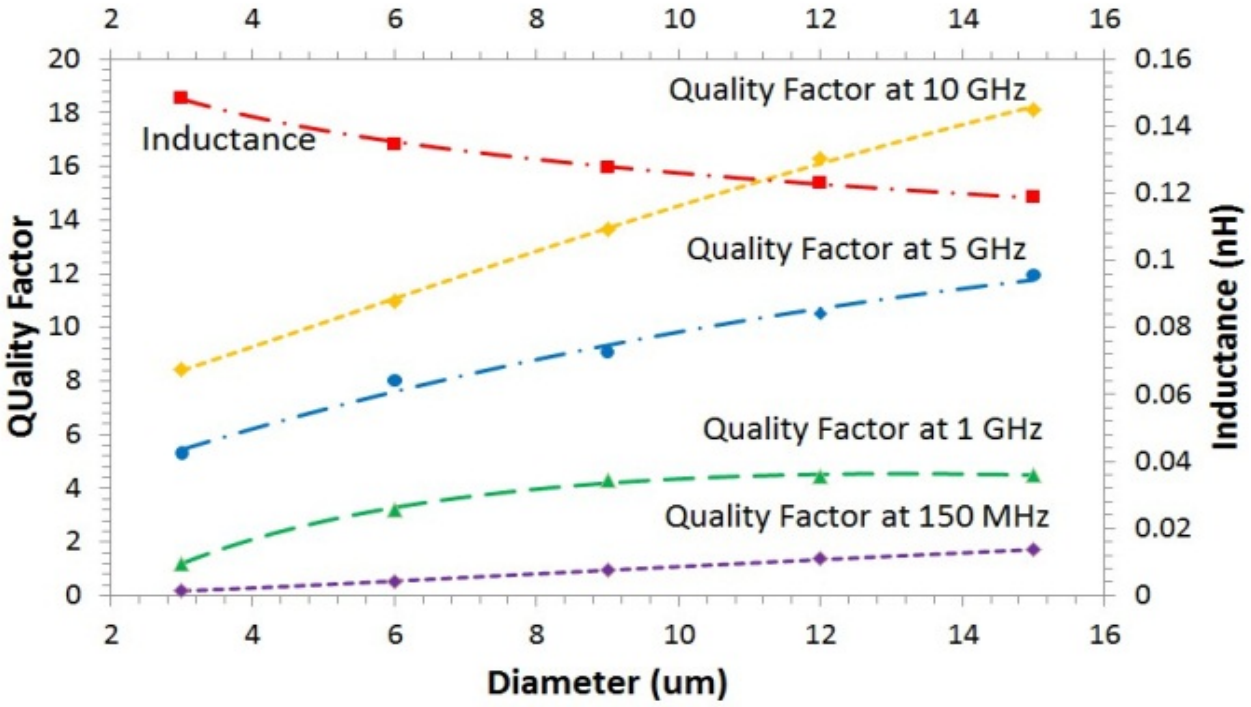
- $L \propto H\ln(H)$
- $Q \propto \ln(H)$
- f_{SR} decreases from over 250 GHz to 100 GHz

Substrate Conductivity (σ)



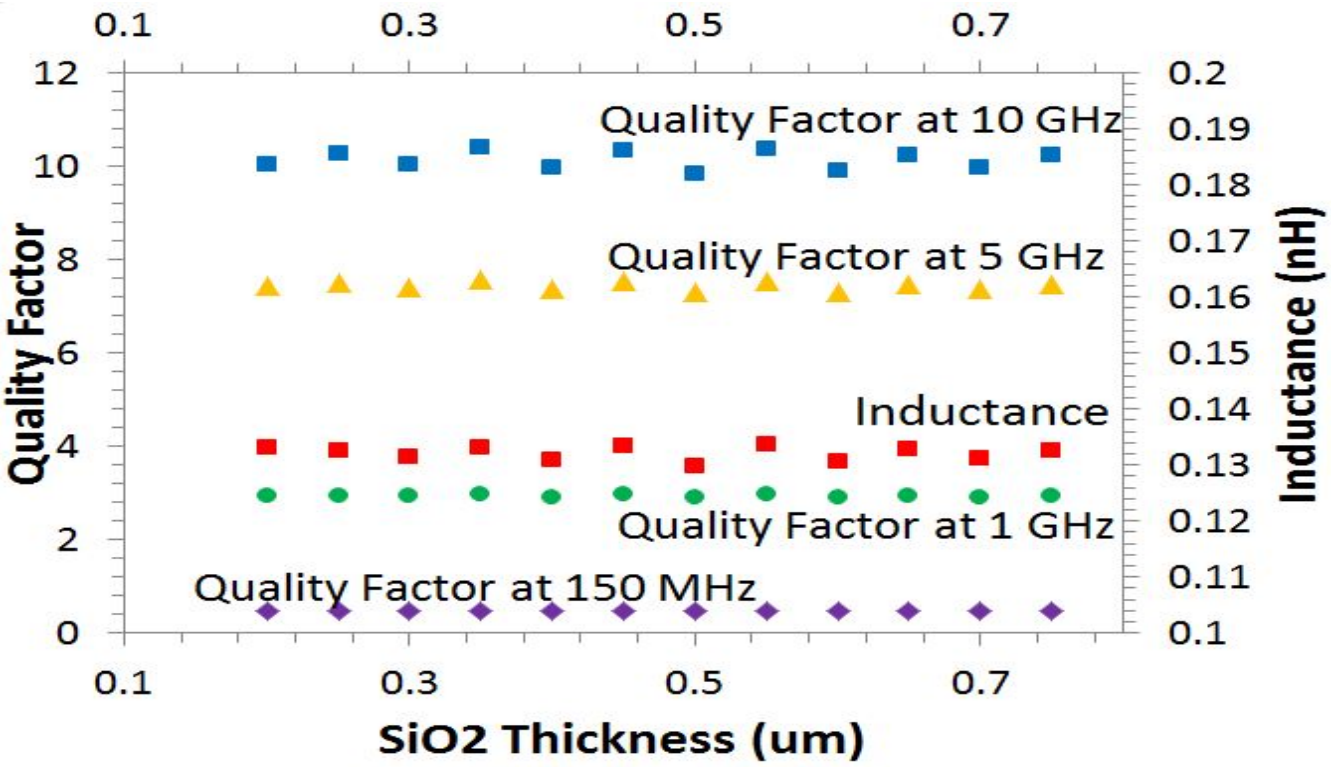
- L remains almost constant
- Q
  - ✓ Constant at low frequency
  - ✓ Decreases quadratically at high frequency
- f_{SR} decreases from over 200 GHz to 60 GHz

Diameter (D)



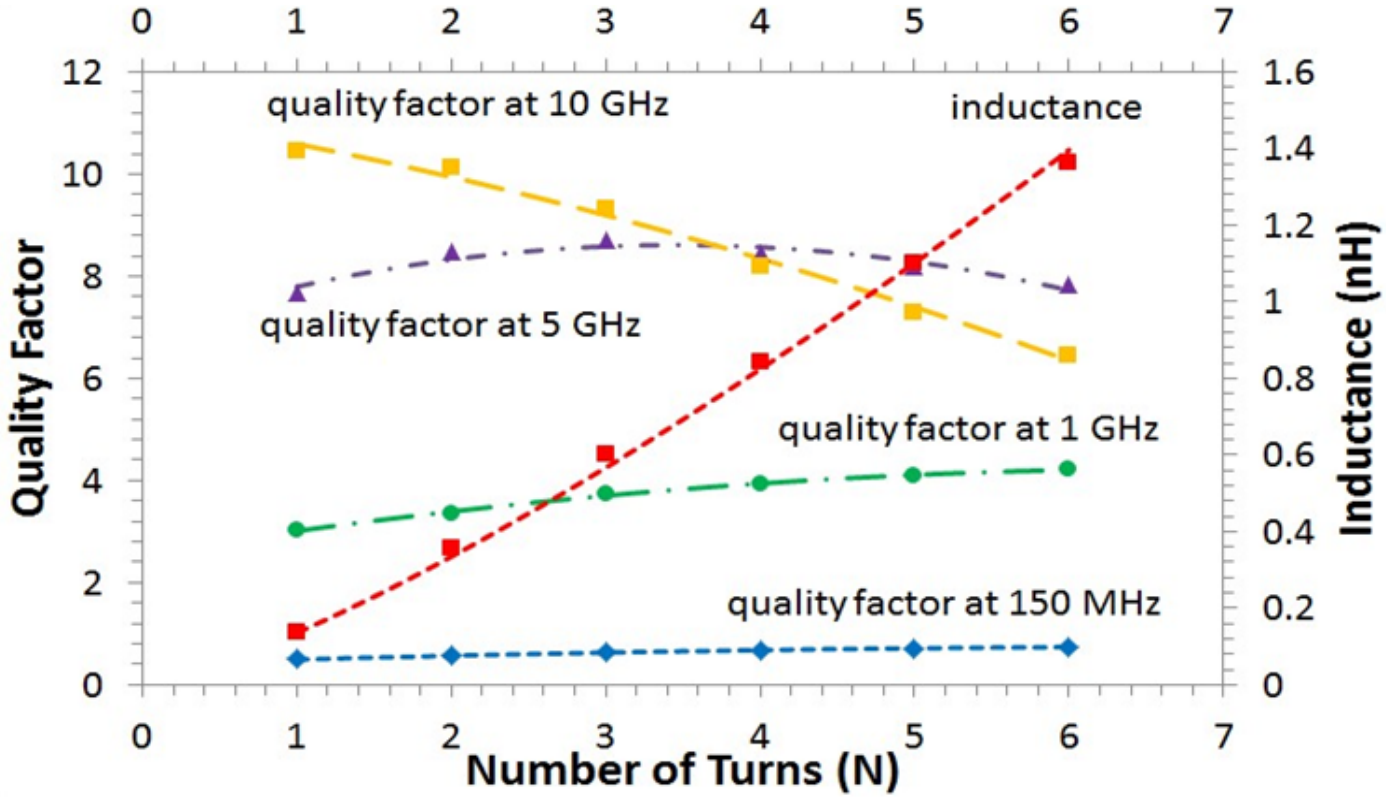
- $L \propto \ln(H/D)$
- $Q \propto D^k$ (k decreases with f)
- f_{SR} is almost constant and is over 200 GHz

Liner Thickness (d)



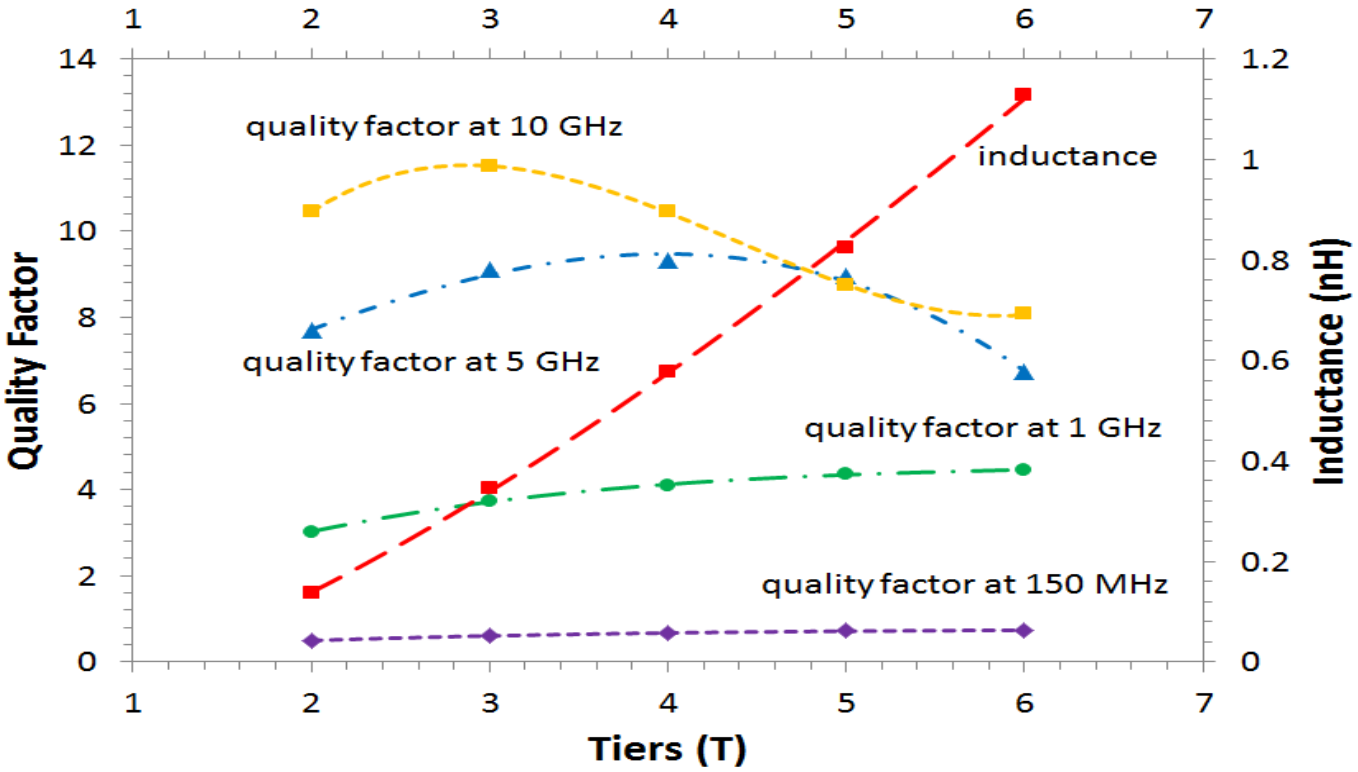
- Q, L and f_{SR} remain almost constant

Number of Turns (N)



- $L \propto N^k$ (k=1.3)
- Q has a peak (critical number of turns)
- f_{SR} decreases from over 200 GHz to 40 GHz

Number of Tiers (T)



- L ∝ Tln(T)
- Q has a peak (critical number of tiers)
- f_{SR} decreases from over 200 GHz to 38 GHz

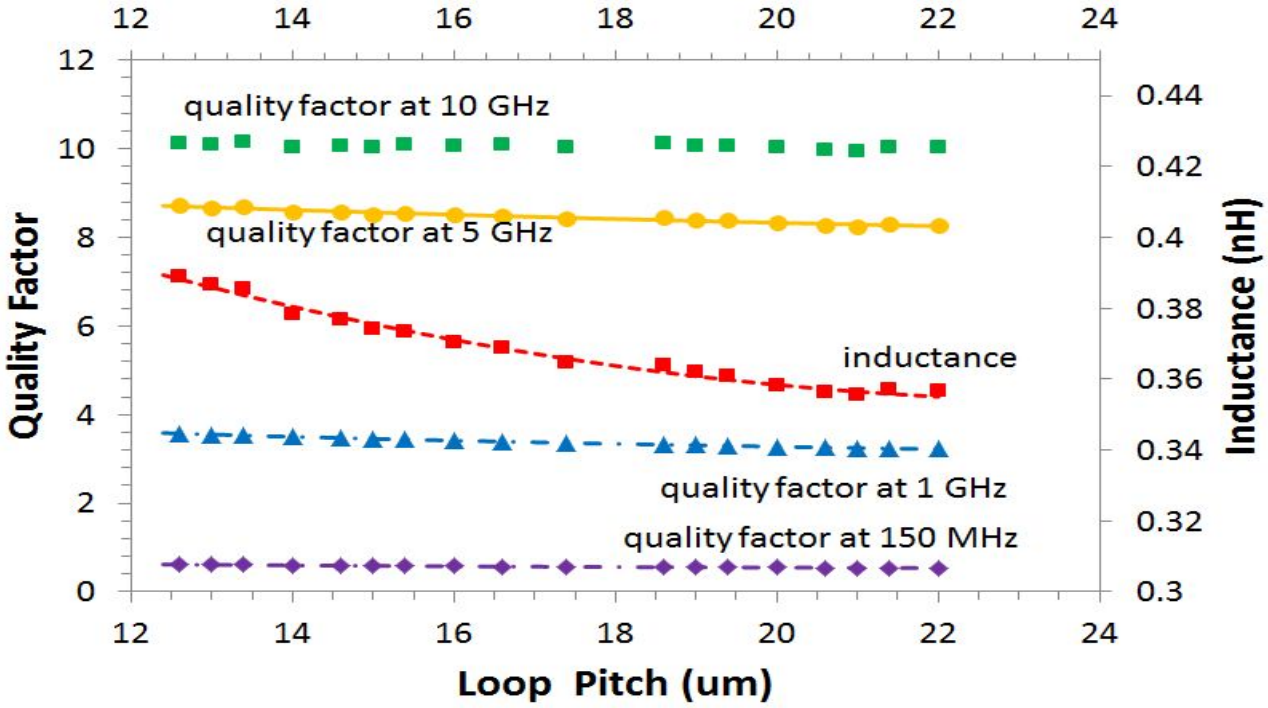
Critical Number of Turns and Tiers

T	2	3	4	5
N_c	3	1	1	1
Q_{max}	8.77	9.11	9.32	8.95

At 5 GHz

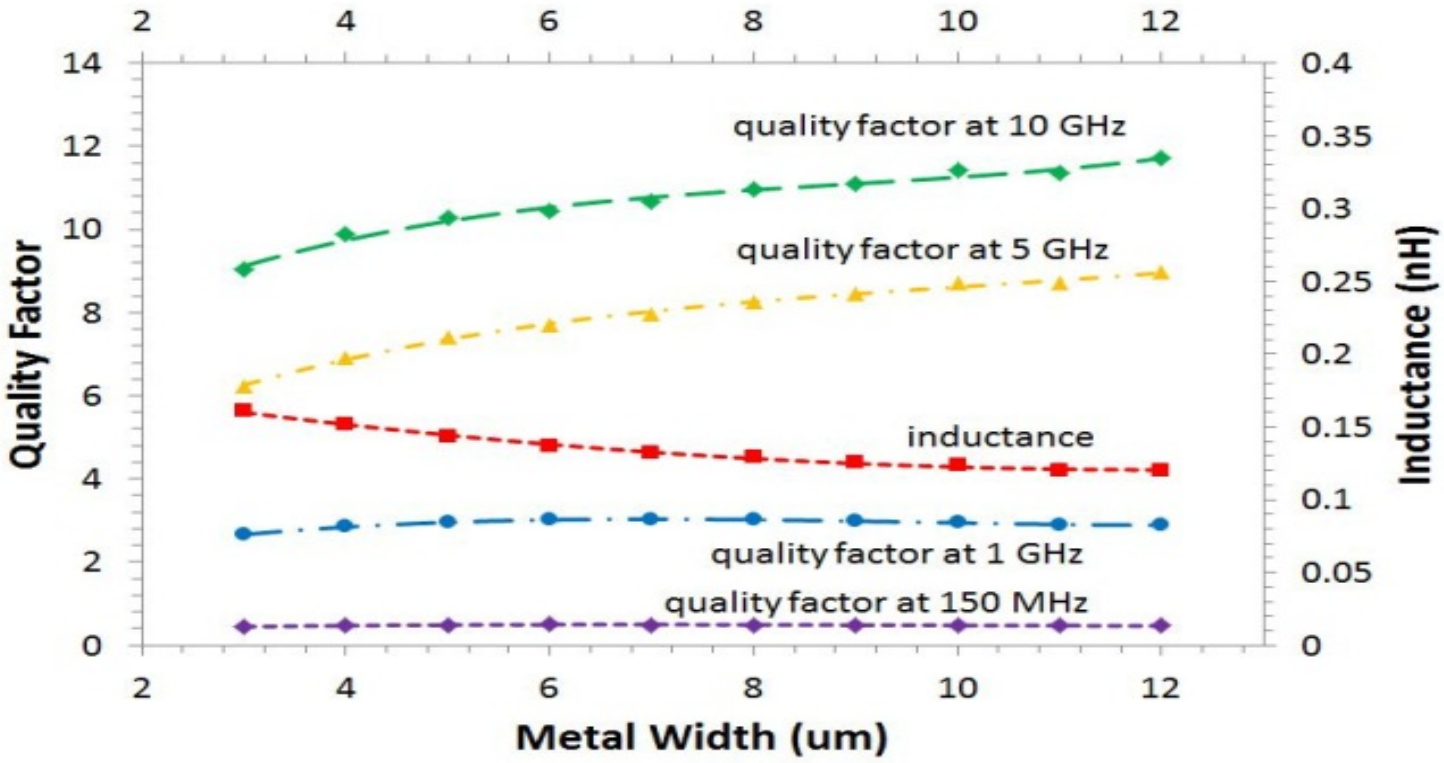
N	1	2	3	4	5
T_c	4	2	2	2	2
Q_{max}	9.32	8.5	8.77	8.6	8.23

Loop Pitch (P)



- L decreases quadratically
- Q gradually decreases
- f_{SR} doesn't change much

Metal Width (W)



- L decreases with W
- Q
  - ✓almost constant at low frequency
  - ✓increases at higher frequency
- f_{SR} doesn't change significantly

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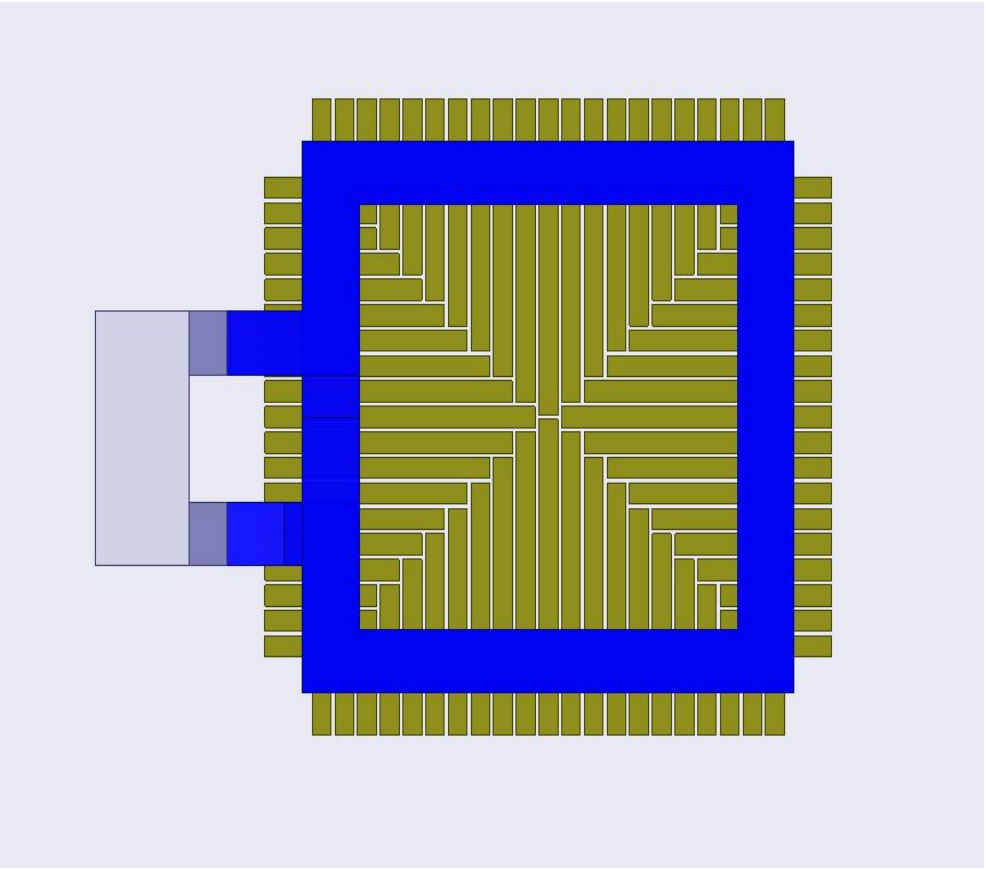
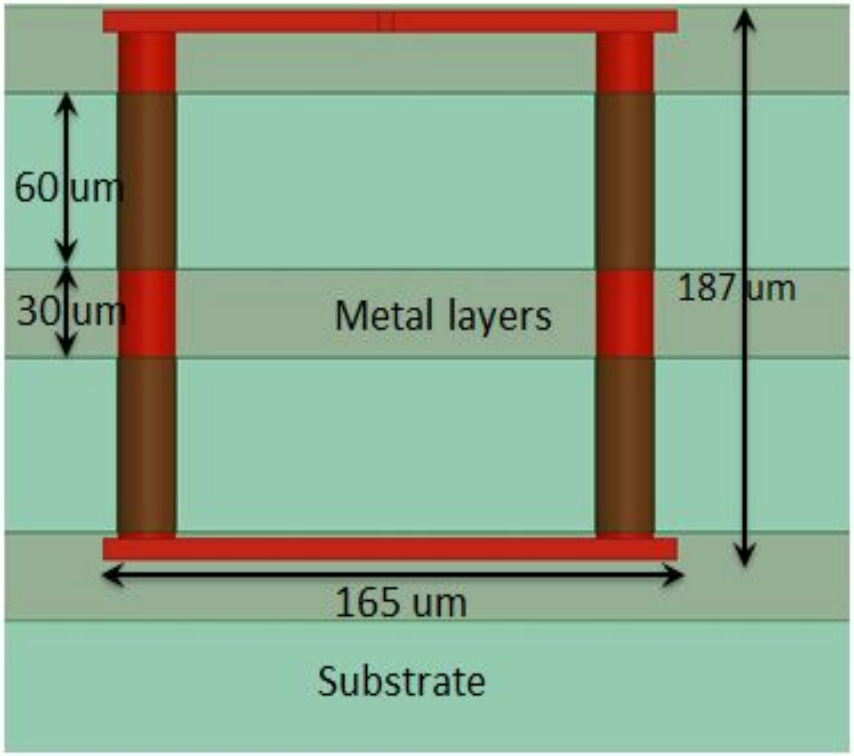
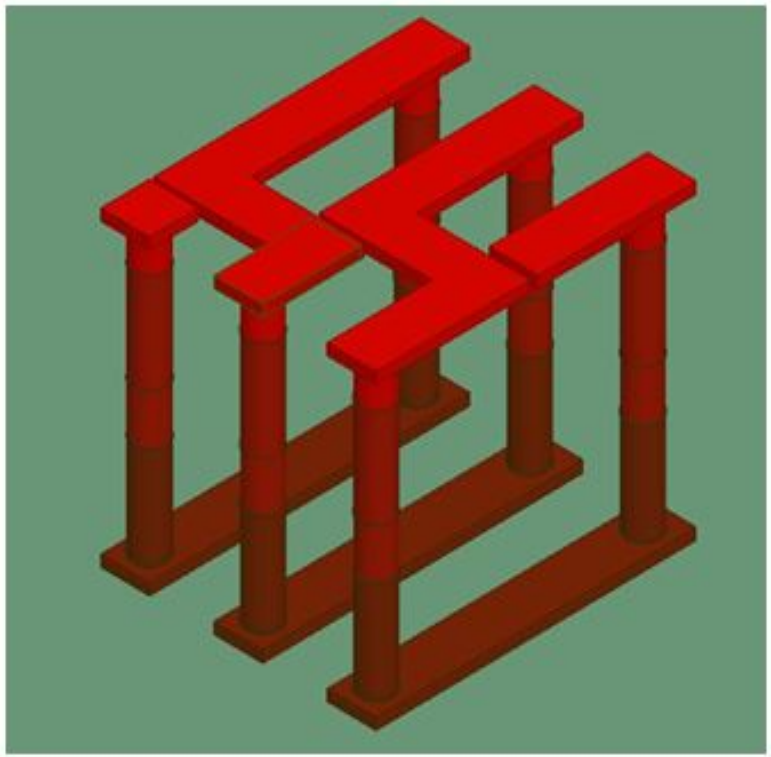
Spiral Inductor – Reference Design



- The substrate height is 300 um.
- The patterned ground shield (PGS) is constructed 5 um below the spiral inductor.
- The PGS uses 10 um metal width with 1 um pitch.
- Outer diameter=336 um
- Pitch = 5 um

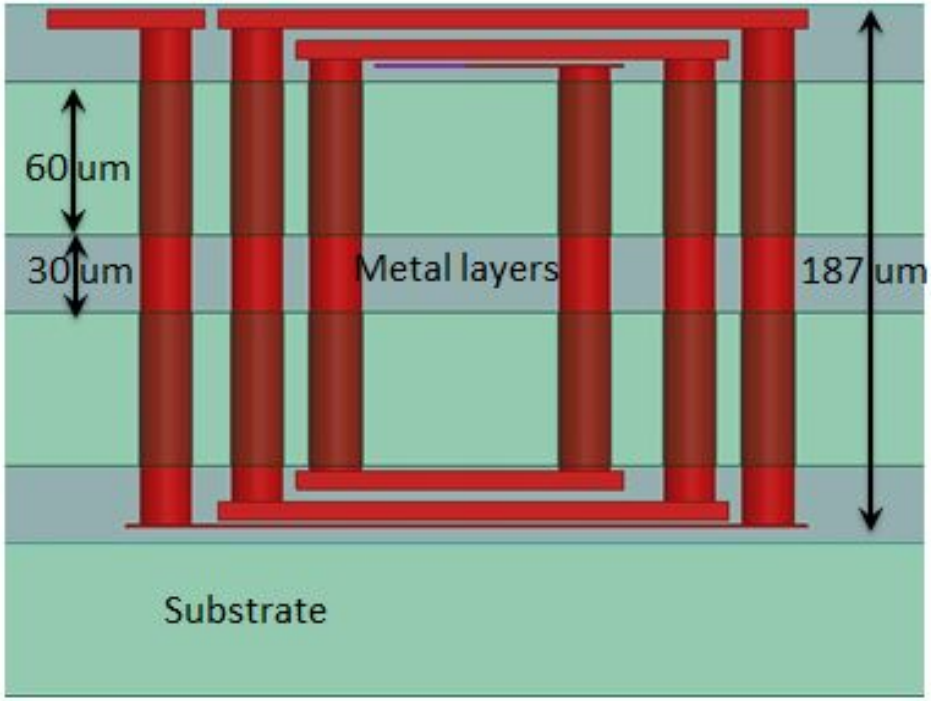
Toroidal TSV Inductor

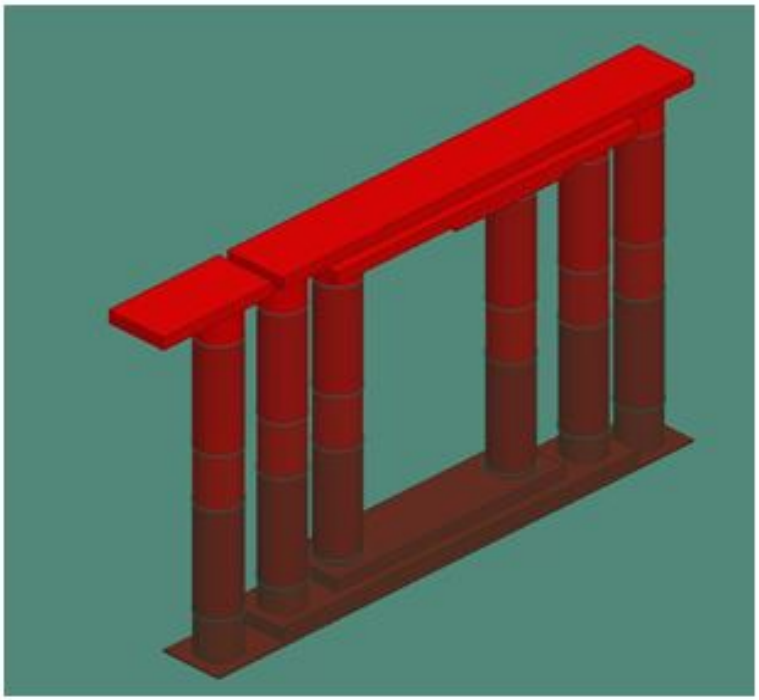




Top metal layers is used i.e., M9
Loop pitch = 5 um, 3 turns

Vertical Spiral Inductor





Three top metal layers are used i.e., M7, M8 and M9

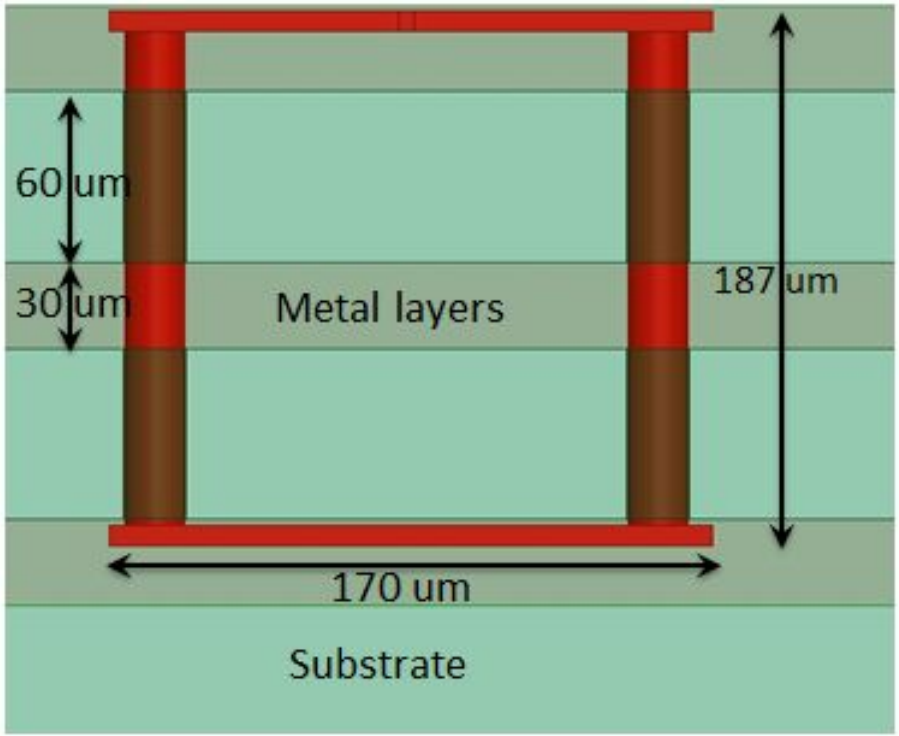
Comparison Summary

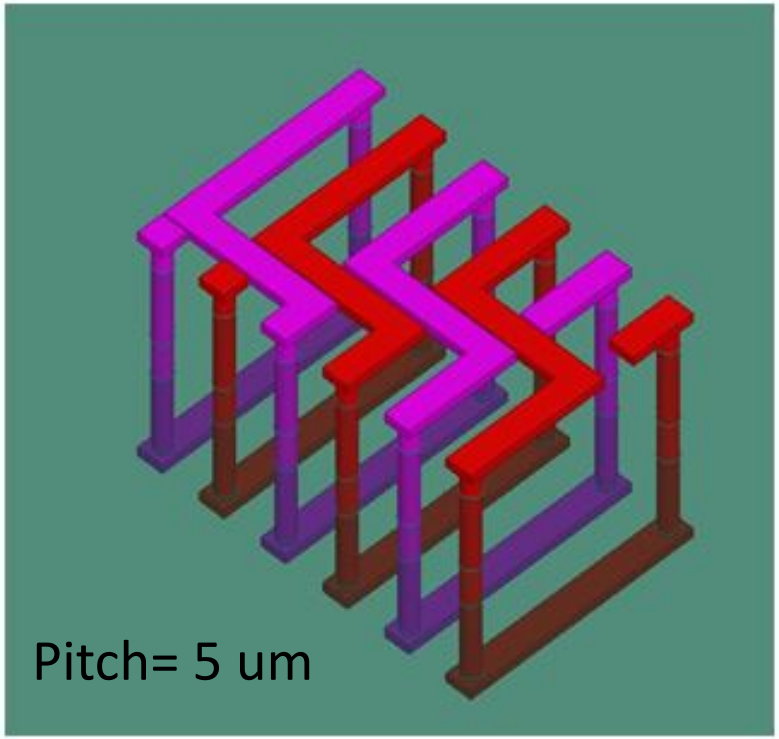
Type	Spiral	Toroidal	Vertical spiral
L(nH)	1.73	1.72	1.73
$R_{dc}(m\Omega)$	178	170	232
$R_{ac}(m\Omega)$	404	254	354
Q	5.4	8.5	6.1

Spiral Inductor Pair – Reference Design

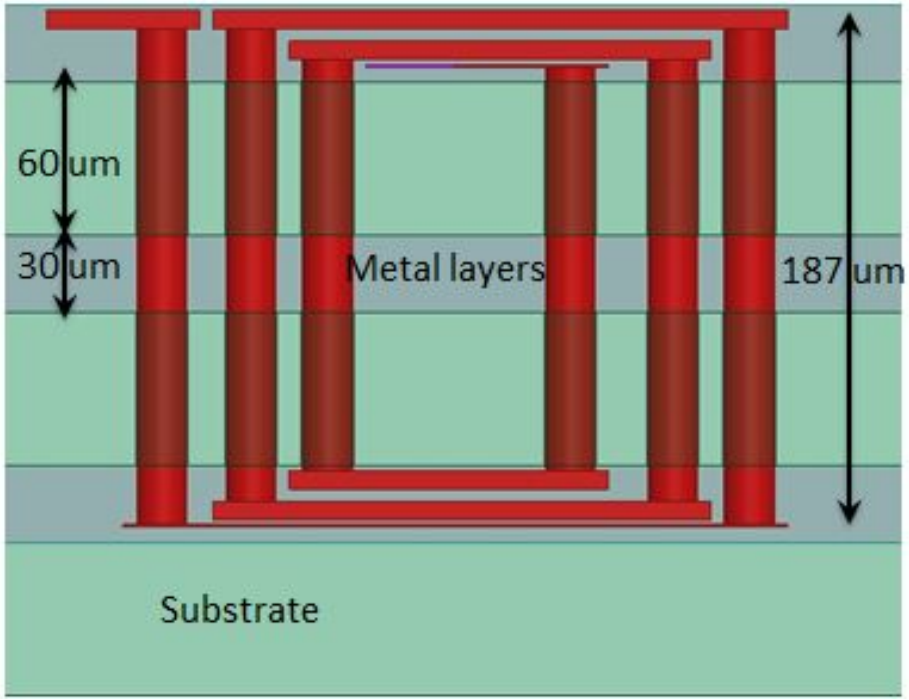
- The coupled inductor pair is implemented using M8 and M9 (one on each layer).
- Each inductor has 2 turns, and the diameter is 350 um.
- Pitch= 5 um

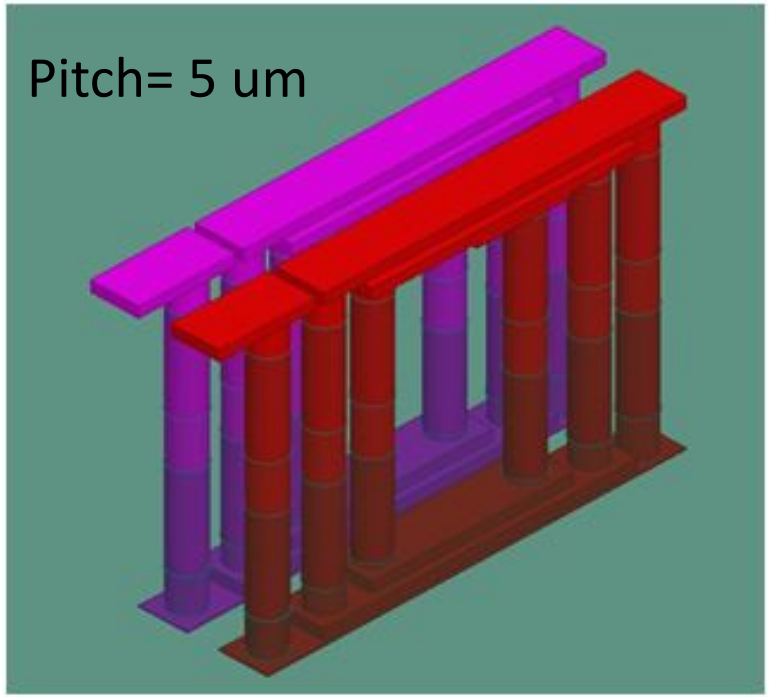
Toroidal Inductor Pair





Vertical Spiral Inductor Pair





Comparison Summary

Type	Spiral	Toroidal	Vertical spiral
k	0.81	0.71	0.57
L_p(nH)	1.85	1.86	1.84
L_s(nH)	1.85	1.86	1.84
R_{p_dc}(mΩ)	178	246	312
R_{s_dc}(mΩ)	177	246	312
R_{p_ac}(mΩ)	630	358	494
R_{s_ac}(mΩ)	808	356	489
Q_p	3.7	6.5	4.7
Q_s	2.9	6.5	4.6

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Circuit Design Settings

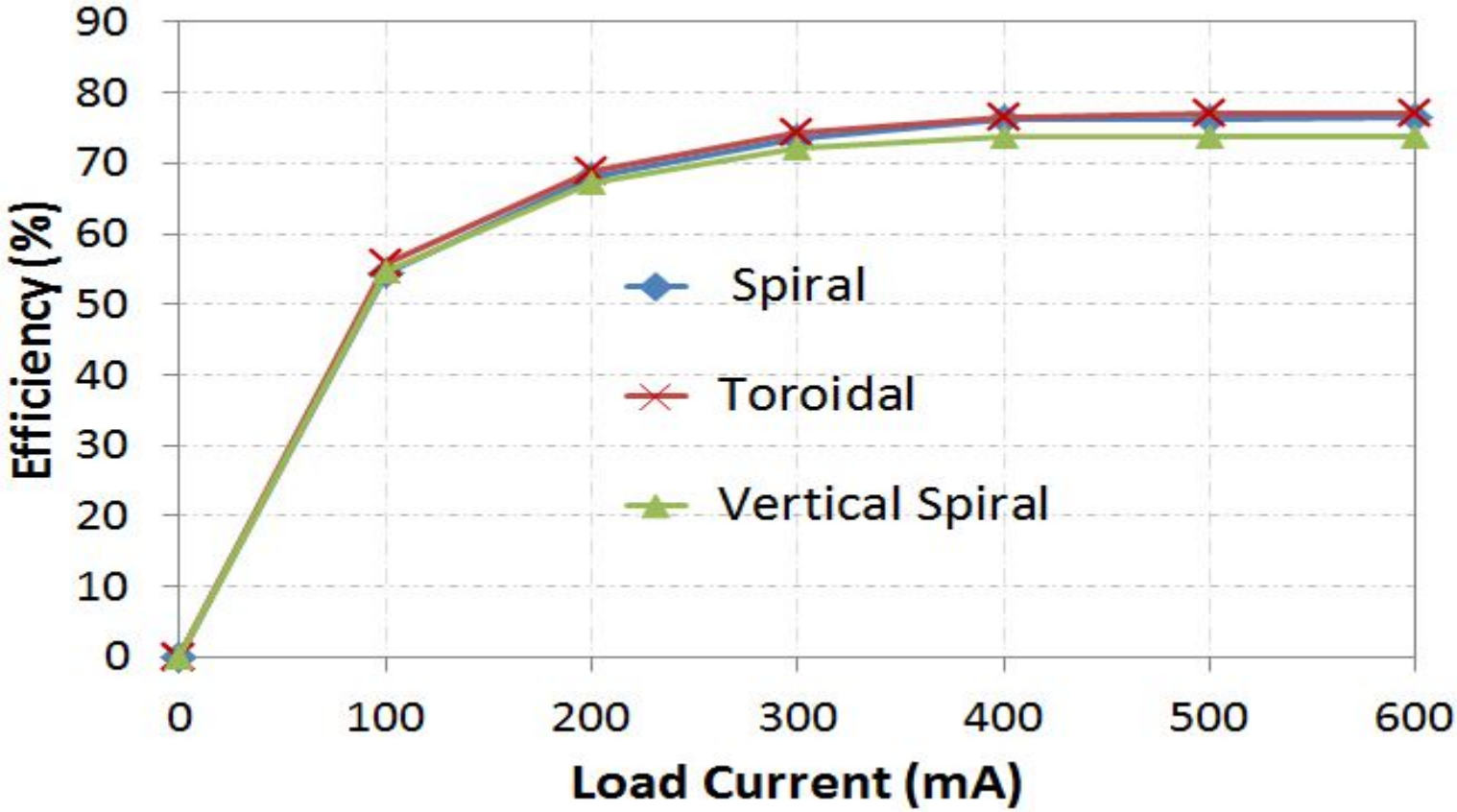
- Design specs
  - V_{in} = 1.5V
  - V_{out} = 1.2V
  - Max voltage droop=15%
  - Frequency of operation = 200MHz
- The designs are implemented in a commercial custom IC design environment with a 45nm process design kit.
- The inductors are embedded in the designs using S-parameter models
  - extracted from an industrial 3D full-wave EM simulation tool
  - in the frequency range of DC to 10 GHz.
- Six designs implemented
  - buck converters with conventional spiral inductor, toroidal TSV inductor and vertical spiral TSV inductor
  - interleaved converters with magnetic coupling using these three inductors
- DC current load assumed for all designs

Buck Converter Results

Type	Spiral	Toroidal	Vertical spiral
Peak efficiency (%)	76.6	77.1	74.0
Ripple (mV)	45	45	46
Inductor area (um^2)	225,792(1)	64,999(1/3.5x)	53,120(1/4.3x)

- Optimal load is around 400 mA for all designs
- The peak efficiency is slightly higher for the toroidal TSV inductor and lower for the vertical spiral TSV inductor
  - ✓ due to the difference in R_{dc}
- The output voltage ripple for all the cases are also almost the same
  - ✓ due to the same inductance and capacitance values in all the cases.
- The area for all inductors is measured by the total routing resource occupied
- For TSV inductors, the area also includes the substrate surface occupied by the TSVs

Efficiency v.s. Load Plot

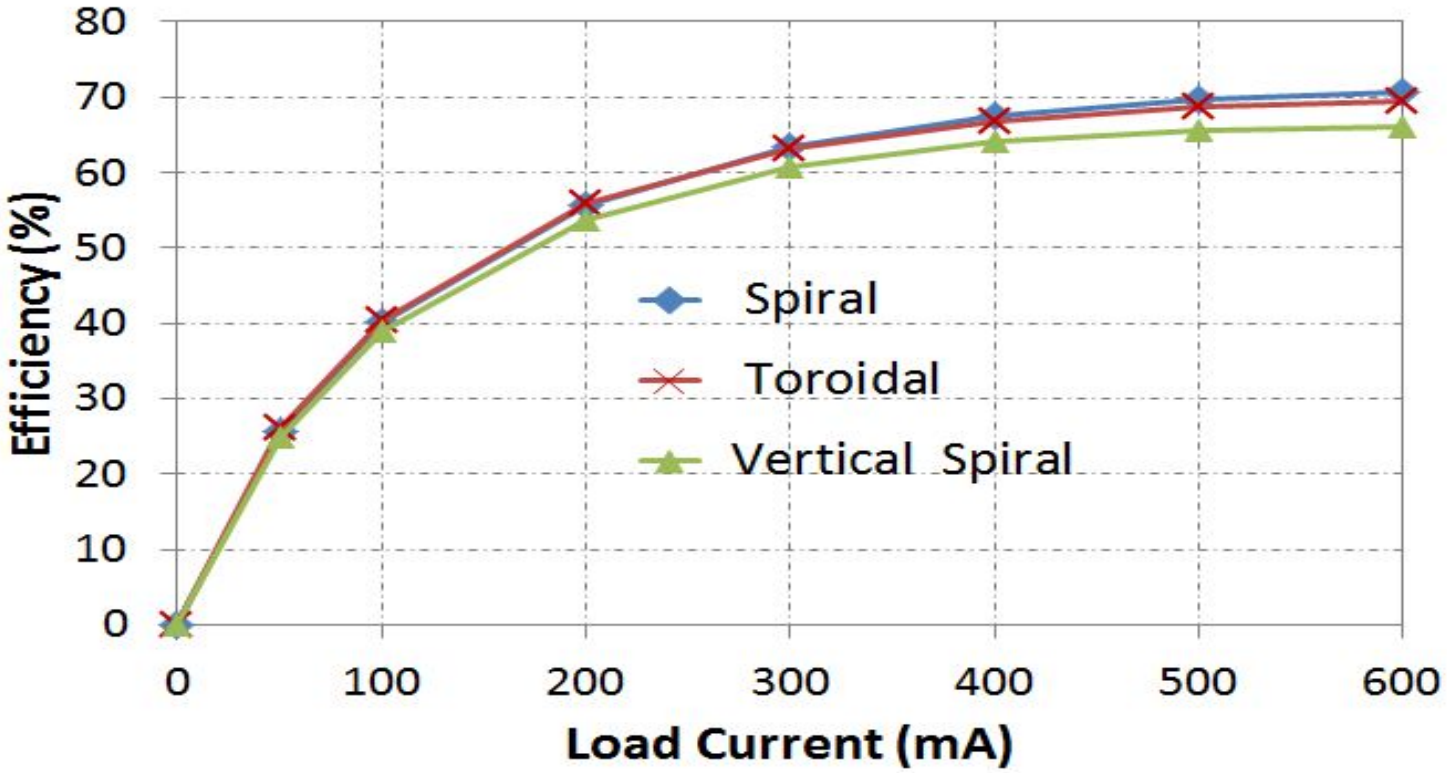


Interleaved Converter Results

Type	Stacked pair	Toroidal TSV pair	Vertical spiral TSV pair
Peak efficiency(%)	70.7	69.4	66.0
Ripple (mV)	17 (1)	10 (58.8%)	10 (58.8%)
Inductor area (um^2)	367,500(1)	147,208(1/2.5x)	115,438(1/3.2x)

- Optimal load is around 450 mA for all designs
- Peak efficiency difference due to R_{dc}
- Ripple difference due to R_{ac}

Efficiency v.s. Load Plot



Conclusions

- Impacts of process and geometry parameters on TSV inductors are discussed
- On-chip DC-DC converters are implemented using 45 nm process with different TSV inductor configurations
  - Inductor area reduction of up to 4.3x (3.2x) over spiral inductor implementations for buck (interleaved) converters
  - Ripple reduction of up to 58.8% over spiral inductor implementations for interleaved converters